DVB-S Demodulator IP Core Specification

Release Information

Name	DVB-S Demodulator IP Core
Version	2.0
Build date	2020.12
Ordering code	ip-dvb-s-demodulator
Specification revision	r1884

Features

The DVB-S Demodulator IP Core is a QPSK demodulator and channel decoder for digital satellite television transmissions to the European Broadcast Union ETSI EN 300 421 standard. The IP Core receives I and Q signals from ADC, digitally demodulates this signal, implements the complete DVB FEC decoding and descrambling function. The output is in the form of MPEG2 transport stream data packets.

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The DVB-S Demodulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the DVB-S Demodulator IP Core block diagram.

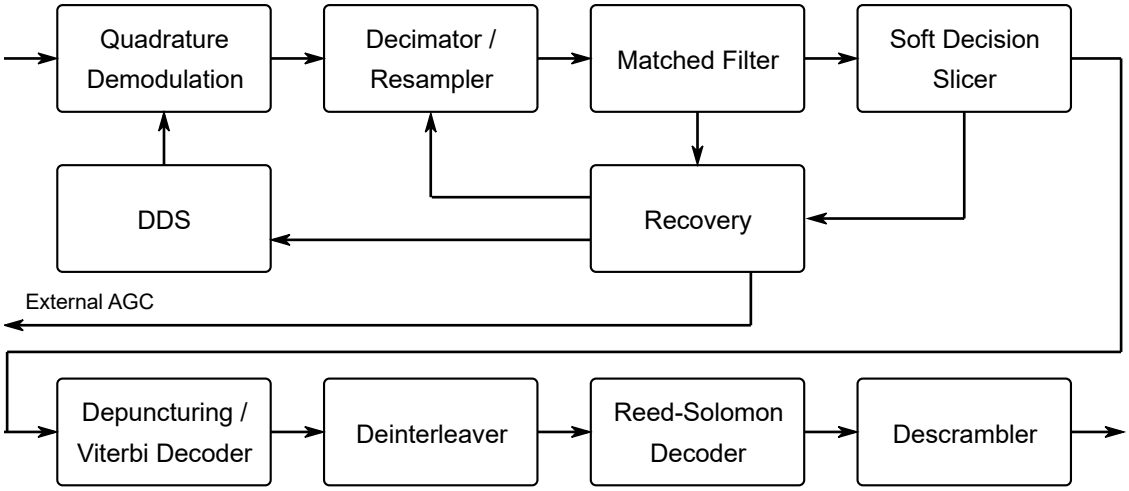

Figure 1. The DVB-S Demodulator IP Core block diagram

Port Map

Table 1 describes the ports of the DVB-S Demodulator IP Core.

Table 1. The DVB-S Demodulator port map description

Port	Width	Description
iclk	1	System clock frequency
icode	3	Code rate: 0 - 1/2 1 - 2/3 2 - 3/4 3 - 5/6 4 - 7/8 5 - Blind search
idati	W_ADC	Input data (I-channel) at zero IF
idatq	W_ADC	Input data (Q-channel) at zero IF
imixer_freq	32	Setup input intermediate frequency
ingc1_ref	10	Setting the reference level of external AGC
ingc2_gain	8	Adjust the speed of adjustment of internal AGC
ingc2_max	16	Set maximum level of AGC
ingc2_min	16	Set minimum level of AGC
ingc2_ref	10	Setting the reference level of internal AGC

ingc3_lag	3	Setting the reference level of internal AGC
ingc3_ref	8	Setting the reference level of internal AGC
irecoverc_lag	5	Selecting band loop filter to adjust carrier frequency
irecoverc_lead	5	Selecting band loop filter to adjust carrier frequency
irecoverc_limit	5	Setting the range of changes to adjust carrier frequency
irecoverc_wen	1	Enables the loop filter to adjust carrier frequency
irecoverc_lag	5	Selecting band loop filter to adjust symbol frequency
irecoverc_lead	5	Selecting band loop filter to adjust symbol frequency
irecoverc_limit	5	Setting the range of changes to adjust symbol frequency
irecoverc_wen	1	Enables the loop filter to adjust symbol frequency
iresampler_cicgain	6	CIC Filter gain control
iresampler_div	12	CIC Filter decimation ratio (when iresampler_src = 1)
iresampler_freq	32	Fractional decimation ratio (when iresampler_src = 0)
iresampler_src	1	Disables fractional decimation
irst	1	The IP Core synchronously reset when irst is asserted high.
itrsh	8	Setting the soft decision slicer threshold
ongc1_det	1	External AGC detector output
orecoverc_acc	32	Carrier frequency error value
orecoverc_lock	2	Carrier frequency lock indicator
ors_dat	8	RS Codec data (before descrambler)

ors_decfail	1	RS Codec decoding failed
ors_err	8	RS Codec error mask
ors_numerr	5	RS Codec number of detected errors in single block
ors_sop	1	RS Codec start of decoding block
ors_val	1	RS Codec valid signal
osmb_dati	8	Output constellation (I-channel)
osmb_datq	8	Output constellation (Q-channel)
osmb_val	1	osmb_dati/osmb_datq valid signal
ostate	2	Code rate lock indicator
osync	1	0x47 preamble correct acquisition
ots_dat	8	Output (Information) data
ots_sop	1	ots_dat sync signal
ots_val	1	ots_dat valid signal
ovitdec_dat	1	Viterbi decoder output data
ovitdec_err	2	Viterbi decoder error mask
ovitdec_val	1	ovitdec_dat valid signal

IP Core Operation Description

Key features of the IP Core:

- Synchronous, high-speed algorithm of QPSK demodulation
- Symbol rate to 1/2 of the system clock frequency
- Symbol rate range 200 MSymbols/s to 50 KSymbols/s (for Xilinx ZCU102 board)
- Fully digital reference frequencies recovery and signal demodulation
- High performance Viterbi Decoder, Deinterleaver and Reed-Solomon Decoder
- Fixed delay in demodulator

IP Core Parameters

Table 2 describes the DVB-S Demodulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-S Demodulator IP Core parameters description

Parameter	Description
W_ADC	**ADC Width**. Width of the Demodulator input samples from ADC (**idati/idatq**).

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-S Demodulator IP Core measurement results.

Table 3. The DVB-S Demodulator performance

IP Core parameters	**FPGA type**	
	Resource	**Performance**
W_ADC = 14	Xilinx ZCU102 board, XCZU9EG	
	2090 CLBs (6%) 11 18K RAM blocks (1%) 14 DSP (18x18) (1%)	410.0 MHz System Clock Rate 205.0 MSymbols/s QPSK 188.92157 Mbit/s with Code Rate 1/2 251.89542 Mbit/s with Code Rate 2/3 283.38235 Mbit/s with Code Rate 3/4 314.86928 Mbit/s with Code Rate 5/6 330.61275 Mbit/s with Code Rate 7/8

IP Core Interface Description

Figure 2 shows an example of the waveform of the output interface. Handshake port **ots_val** controls output dataflow. Output data is read from the output **ots_dat** only when **ots_val** is equal to logical one ("1").

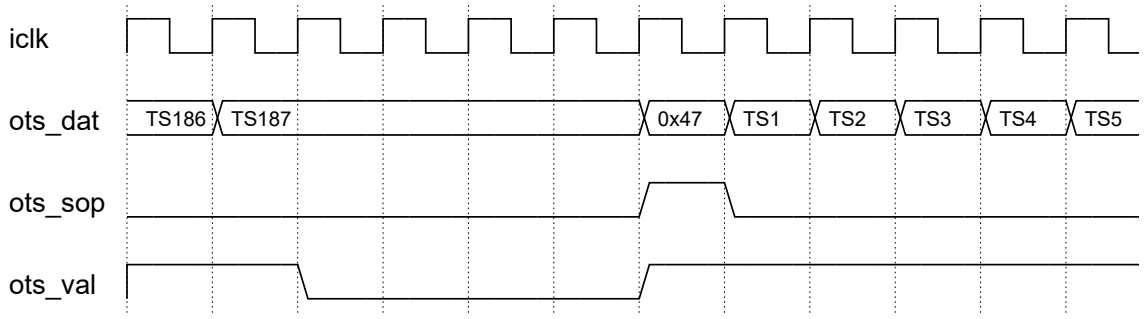

Figure 2. The timing diagram of the IP Core output interface.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

Modemica OU

Sepapaja 6, Tallinn, 15551, Estonia

Tel.: +39-350-0080495

E-mail: info@modemica.com

Skype: fpgahelp

website: https://www.modemica.com

Revision history

Version	Date	Changes
2.0	2020.12.01	New architecture with twice bigger demodulation bandwidth
1.2	2017.07.11	Changed output interface. Added carrier frequency error indication ports
1.1	2016.08.09	Changed output interface. Added decoding errors indication ports
1.0	2015.06.30	Official release