DVB-C Modulator IP Core Specification

Release Information

Name	DVB-C Modulator IP Core
Version	5.1
Build date	2021.03
Ordering code	ip-dvbc-modulator
Specification revision	r1884

Features

The IP core is full-featured 32-channel digital DVB-C modulator and is fully compatible with the standard:

- ETSI EN 300 429 (v1.2.1)

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The DVB-C Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the DVB-C Modulator IP Core block diagram for one channel.

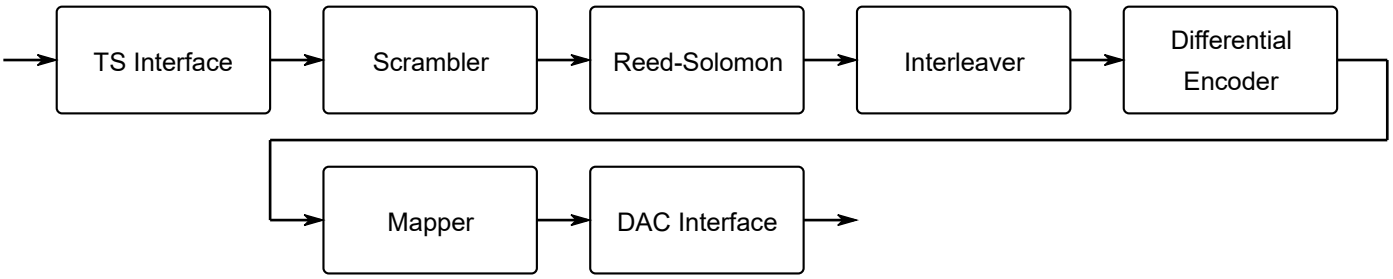

Figure 1. The DVB-C Modulator IP Core block diagram

The DVB-C modulator consists of an input TS interface (**TS Interface**), a scrambler (**Scrambler**), a Reed-Solomon encoder (**Reed-Solomon**), an interleaver (**Interleaver**), a differential

encoder (**Differential Encoder**), a constellation mapper (**Mapper**) and a MAX5861/MAX5862 interface (**DAC Interface**).

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-C Modulator IP Core.

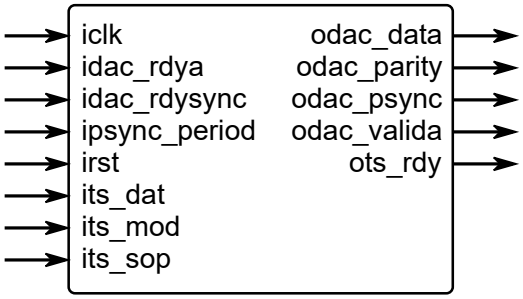

Figure 2. The DVB-C Modulator port map

Table 1. The DVB-C Modulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idac_rdya	2	The RDYA signal from the DAC. Two bits are {second in time, first in time} IDDR outputs.
idac_rdysync	2	The RDYSYNC signal from the DAC. Two bits are {second in time, first in time} IDDR outputs.
ipsync_period	8	Number of timeslots of the DAC.
irst	1	The IP Core synchronously reset when irst is asserted high.
its_dat	256	TS data for 32 parallel DVB-C channels (1 channel = 8 bits).
its_mod	96	Modulation for channel N = its_mod[3*N+2 : 3*N]: 0 - 16-QAM 1 - 32-QAM 2 - 64-QAM 3 - 128-QAM 4 - 256-QAM
its_sop	32	Input sync-word byte markers (0x47 TS) for 32 parallel DVB-C channels.

odac_data	20	The DAC DATA (constellation symbols) for ten parallel ODDR primitives.
odac_parity	2	The DAC PARITY data. Two bits are {second in time, first in time} ODDR inputs.
odac_psync	2	The DAC PSYNC data. Two bits are {second in time, first in time} ODDR inputs.
odac_valida	2	The DAC VALIDA data. Two bits are {second in time, first in time} ODDR inputs.
ots_rdy	32	Ready to accept TS data for 32 parallel DVB-C channels.

IP Core Parameters

Table 2 describes the DVB-C Modulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-C Modulator IP Core parameters description

Parameter	Description
There are no parameters available to change	

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-C Modulator IP Core measurement results.

Table 3. The DVB-C Modulator performance

IP Core parameters	FPGA type	
	Resource	**Performance**
MAX_TS = 32	Xilinx ZCU102 board, XCZU9EG	
	2815 CLBs (9%) 64 18K RAM blocks (2%) 0 DSP (18x18) (0%)	128+ MHz System Clock 32 DVB-C channels up to 7.5 MSymbols/s at 256-QAM

IP Core Interface Description

The DVB-C Modulator IP Core supports 32-channel operating mode with the MAX5861/MAX5862 DAC and allows to output spectrum 0 MHz to 1100 MHz with bandwidth 2 MHz to 7.5 MHz.

Figure 3 shows the DAC connection diagram.

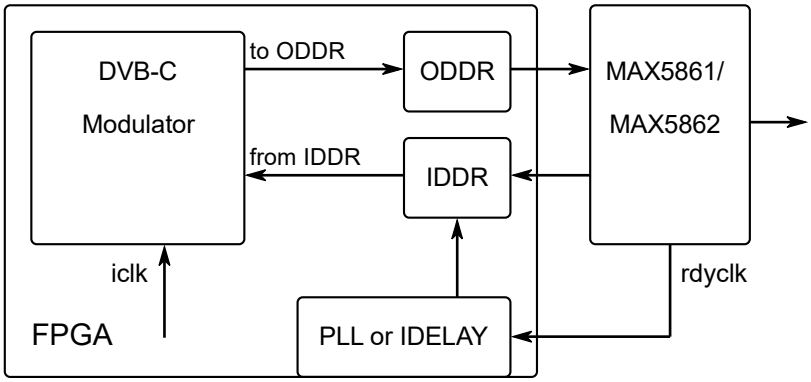

Figure 3. The connection diagram for MAX5861/MAX5862 DAC.

Figure 4 shows an example of the waveform of the input interface. Handshake port **ots_rdy** controls input dataflow. Input data is read from the input **its_dat** only when **ots_rdy** is equal to logical one ("1").

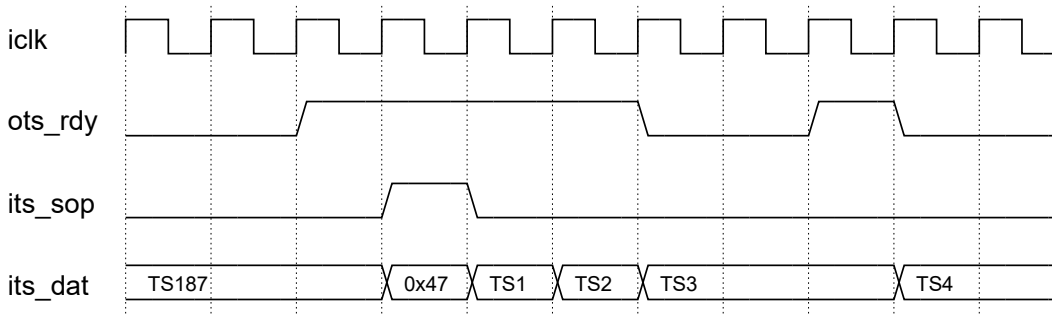

Figure 4. The timing diagram of the IP Core input interface.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

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Revision history

Version	Date	Changes
5.1	2021.03.15	Added independent modulation type control for 32-channel DVB-C
5.0	2021.01.20	32-channel DVB-C for MAX5861 and MAX5862 DAC
4.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
3.1	2015.04.06	Added support for the AD9789 (2400 MSPS RF DAC) and 4-channel operating mode
3.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
2.0	2014.03.17	MER and C/I improvements
1.1	2010.12.22	Maintenance improvements
1.0	2010.12.03	Official release