I.3 40G BCH Encoder/Decoder IP Core Specification

Release Information

Name	I.3 40G BCH Codec IP Core
Version	1.0
Build date	2016.12
Ordering code	ip-i3-40g-bch-codec
Specification revision	r1884

Features

The IP core implements the BCH (3860, 3824) and (2040, 1930) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.975.1 (super-FEC for 2.5G, 10G and 40G optical networks)

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The I.3 40G BCH Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the I.3 40G BCH Encoder IP Core block diagram.

Figure 1. The I.3 40G BCH Encoder IP Core block diagram

The I.3 40G BCH Encoder consists of an outer BCH encoder (**BCH(3860, 3824) outer encoder**), an interleaver module (**Interleaver**) and an inner BCH encoder (**BCH(2040, 1930) inner encoder**).

Figure 2 shows a block diagram of one I.3 40G BCH Decoder IP Core decoding iteration.

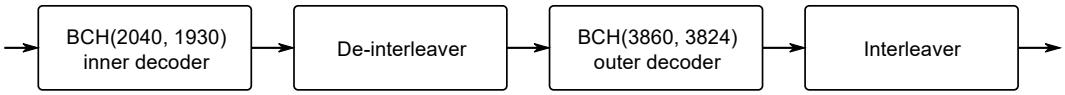

Figure 2. Block diagram of one I.3 40G BCH Decoder IP Core decoding iteration

The I.3 40G BCH Decoder architecture makes it possible to specify a random number of decoding iterations. A decoding iteration consists of an inner BCH decoder (**BCH(2040, 1930) inner decoder**), a deinterleaver module (**De-interleaver**), an outer BCH decoder (**BCH(3860, 3824) outer decoder**) and an interleaver module (**Interleaver**). The interleaver of the latest iteration is not used in **ENDPOINT** mode.

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the I.3 40G BCH Encoder IP Core.

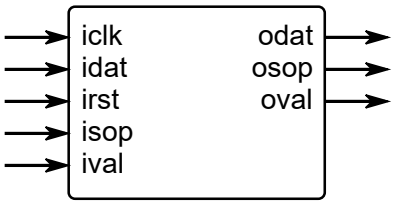

Figure 3. The I.3 40G BCH Encoder port map

Table 1. The I.3 40G BCH Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	256	input (information) data
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of information packet marker
ival	1	input data valid
odat	256	output (encoded) data
osop	1	start of encoded packet marker
oval	1	output data valid

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the I.3 40G BCH Decoder IP Core.

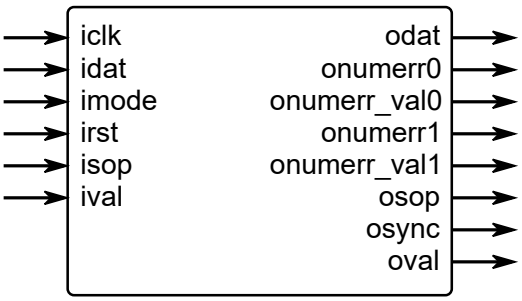

Figure 4. The I.3 40G BCH Decoder port map

Table 2. The I.3 40G BCH Decoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	256	input (encoded) data
imode	1	decoded data output mode: 0 - without correction (bypass) 1 - with error correction
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of coded packet marker
ival	1	input data valid
odat	256	output (decoded) data
onumerr0	5	number of input blocks with errors
onumerr_val0	1	onumerr0 valid
onumerr1	5	number of output blocks with errors
onumerr_val1	1	onumerr1 valid
osop	1	start of decoded packet marker
osync	1	correct isop with FAS input
oval	1	output data valid

IP Core Operation Description

The I.3 40G BCH Encoder/Decoder IP Core is in full accordance with the recommendation ITU-T G.975.1 (02/2004) "Appendix I. Super FEC schemes. I.3 Concatenated BCH super FEC codes". The IP Core is designed for operation with the OTN OTU3 linear stream at 40-46 Gbps in fiber optic communication systems. The I.3 40G BCH Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.975.1 I.3
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 5 cycles
- Decoding delay of a single iteration of decoding (inner decoder - deinterleaver - outer decoder - interleaver) - 1679 cycles (9.9 us)
- Decoding delay of 3 iterations is 5037 cycles (29.7 us)

IP Core Parameters

Table 3 describes the I.3 40G BCH Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The I.3 40G BCH Encoder/Decoder IP Core parameters description

Parameter	Description
ITER	number of decoding iterations
MODE	IP Core configuration: "ENDPOINT" or "REPEATER"

For example:

- ITER = 3 and MODE = "REPEATER" means 3 full decoding iteraions in **REPEATER** mode:

idat - inner1 - deint1 - outer1 - inter1 - inner2 - deint2 - outer2 - inter2 - inner3 - deint3 - outer3 - inter3 - odat

- ITER = 3 and MODE = "ENDPOINT" means 3 full decoding iterations in **ENDPOINT** (without inter3):

idat - inner1 - deint1 - outer1 - inter1 - inner2 - deint2 - outer2 - inter2 - inner3 - deint3 - outer3 - odat

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the I.3 40G BCH Encoder IP Core measurement results.

Table 4. The I.3 40G BCH Encoder performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Arria 10 10AX032			
	11059 ALMs (9%) 16 M20K RAM blocks (2%) 0 DSP (18x18) (0%)	-3, Fmax	-2, Fmax	-1, Fmax
		210.0 MHz 53.76 Gbps	240.0 MHz 61.44 Gbps	260.0 MHz 66.56 Gbps
	Xilinx Virtex-7 XC7VX330T			
	5712 Slices (12%) 16 18K RAM blocks (1%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		270.0 MHz 69.12 Gbps	300.0 MHz 76.80 Gbps	330.0 MHz 84.48 Gbps

Table 5 summarizes the I.3 40G BCH Decoder IP Core measurement results.

Table 5. The I.3 40G BCH Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
3 iterations	Altera Arria 10 10AX032			
	108139 ALMs (90%) 309 M20K RAM blocks (35%) 0 DSP (18x18) (0%)	-3, Fmax	-2, Fmax	-1, Fmax
		170.0 MHz 43.52 Gbps	200.0 MHz 51.20 Gbps	220.0 MHz 56.32 Gbps
3 iterations	Xilinx Virtex-7 XC7VX330T			
	46471 Slices (91%) 273 18K RAM blocks (18%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		165.0 MHz 42.24 Gbps	200.0 MHz 51.20 Gbps	220.0 MHz 56.32 Gbps

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 256 bits. The codec throughput of 43.0 Gbps requires a timing frequency of at least 168 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker.

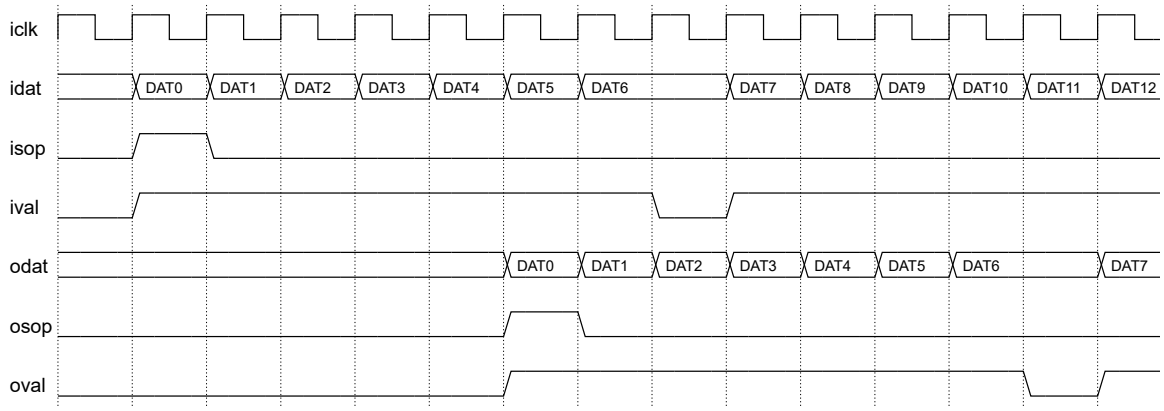

Figure 5. The timing diagrams of the I.3 40G BCH Encoder operation

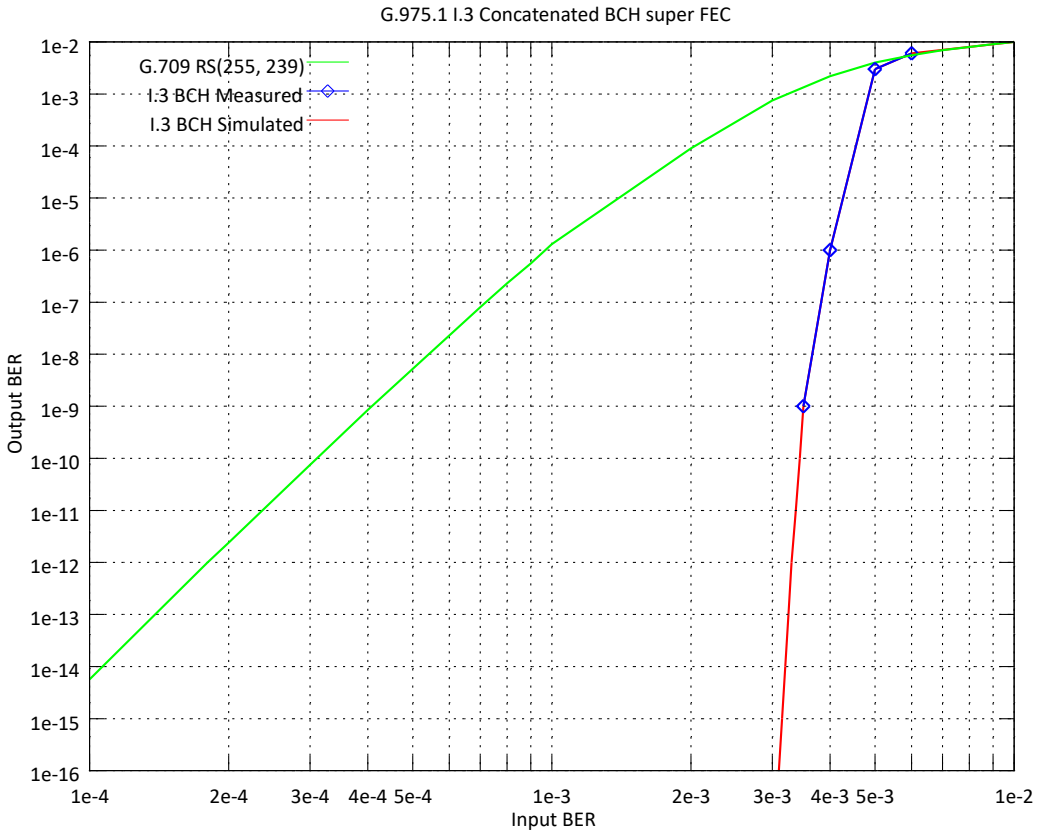

Figure 6. The error-correcting capability of the I.3 40G BCH Decoder

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

Modemica OU

Sepapaja 6, Tallinn, 15551, Estonia

Tel.: +39-350-0080495

E-mail: info@modemica.com

Skype: fpgahelp

website: https://www.modemica.com

Revision history

Version	Date	Changes
1.0	2016.12.27	Official release