I.3 BCH Encoder/Decoder IP Core Specification

Release Information

Name	I.3 BCH Codec IP Core
Version	2.1
Build date	2015.09
Ordering code	ip-i3-bch-codec
Specification revision	r1884

Features

The IP core implements the BCH (3860, 3824) and (2040, 1930) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.975.1 (super-FEC for 2.5G, 10G and 40G optical networks)

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The I.3 BCH Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the I.3 BCH Encoder IP Core block diagram.

Figure 1. The I.3 BCH Encoder IP Core block diagram

The I.3 BCH Encoder consists of a outer BCH encoder (**BCH(3860, 3824) outer encoder**), interleaver module (**Interleaver**) and an inner BCH encoder (**BCH(2040, 1930) inner encoder**).

Figure 2 shows a block diagram of one I.3 BCH Decoder IP Core decoding iteration.

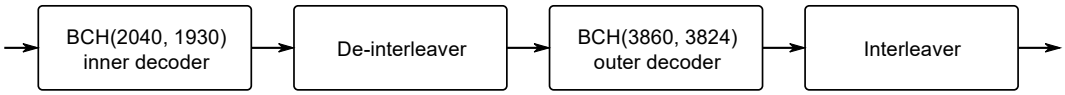

Figure 2. Block diagram of one I.3 BCH Decoder IP Core decoding iteration

The I.3 BCH Decoder architecture makes it possible to specify a random number of decoding iterations. A decoding iteration consists of an inner BCH decoder (**BCH(2040, 1930) inner decoder**), a deinterleaver module (**De-interleaver**), an outer BCH decoder (**BCH(3860, 3824) outer decoder**) and an interleaver module (**Interleaver**). The interleaver of the latest iteration is not used in **ENDPOINT** mode.

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the I.3 BCH Encoder IP Core.

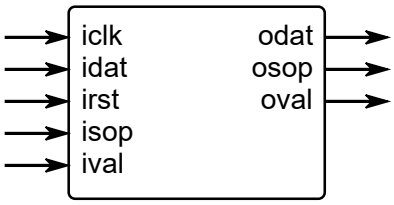

Figure 3. The I.3 BCH Encoder port map

Table 1. The I.3 BCH Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	128	input (information) data
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of information packet marker
ival	1	input data valid
odat	128	output (encoded) data
osop	1	start of encoded packet marker
oval	1	output data valid

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the I.3 BCH Decoder IP Core.

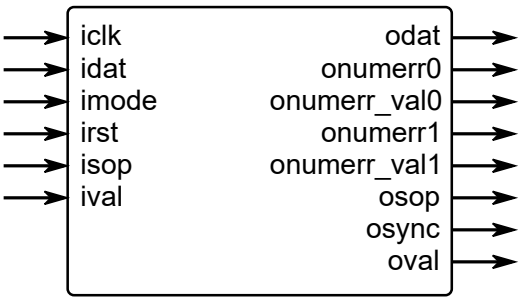

Figure 4. The I.3 BCH Decoder port map

Table 2. The I.3 BCH Decoder port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	128	input (encoded) data
imode	1	decoded data output mode: 0 - without correction (bypass) 1 - with error correction
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of coded packet marker
ival	1	input data valid
odat	128	output (decoded) data
onumerr0	5	number of input blocks with errors
onumerr_val0	1	onumerr0 valid
onumerr1	5	number of output blocks with errors
onumerr_val1	1	onumerr1 valid
osop	1	start of decoded packet marker
osync	1	correct isop with FAS input
oval	1	output data valid

IP Core Operation Description

The I.3 BCH Encoder/Decoder IP Core is in full accordance with the recommendation ITU-T G.975.1 (02/2004) "Appendix I. Super FEC schemes. I.3 Concatenated BCH super FEC codes". The IP Core is designed for operation with the OTN OTU2 linear stream at 10.7 Gbps in fiber optic communication systems. The I.3 BCH Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.975.1 I.3
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 5 cycles
- Decoding delay of a single iteration of decoding (inner decoder - deinterleaver - outer decoder - interleaver) - 3041 cycles (36.4 us)
- Decoding delay of 3 iterations is 9,123 cycles (109.2 us)

IP Core Parameters

Table 3 describes the I.3 BCH Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The I.3 BCH Encoder/Decoder IP Core parameters description	
Parameter	Description
ITER	number of decoding iterations
MODE	IP Core configuration: "ENDPOINT" or "REPEATER"

For example:

- ITER = 3 and MODE = "REPEATER" means 3 full decoding iteraions in **REPEATER** mode:

idat - inner1 - deint1 - outer1 - inter1 - inner2 - deint2 - outer2 - inter2 - inner3 - deint3 - outer3 - inter3 - odat

- ITER = 3 and MODE = "ENDPOINT" means 3 full decoding iterations in **ENDPOINT** (without inter3):

idat - inner1 - deint1 - outer1 - inter1 - inner2 - deint2 - outer2 - inter2 - inner3 - deint3 - outer3 - odat

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the I.3 BCH Encoder IP Core measurement results.

Table 4. The I.3 BCH Encoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Cyclone V 5CEFA7			
	4775 ALMs (9%) 26 M10K RAM blocks (4%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		143.0 MHz 18.3 Gbps	163.0 MHz 20.8 Gbps	203.0 MHz 25.9 Gbps
	Xilinx Virtex-7 XC7VX330T			
	1933 Slices (4%) 15 18K RAM blocks (1%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		266.0 MHz 34.0 Gbps	330.0 MHz 42.2 Gbps	360.0 MHz 46.0 Gbps

Table 5 summarizes the I.3 BCH Decoder IP Core measurement

results.

Table 5. The I.3 BCH Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
3 iterations	Altera Cyclone V 5CEFA7			
	45898 ALMs (82%) 534 M10K RAM blocks (78%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		92.0 MHz 11.7 Gbps	104.0 MHz 13.3 Gbps	120.0 MHz 15.3 Gbps
3 iterations	Xilinx Virtex-7 XC7VX330T			
	18471 Slices (37%) 291 18K RAM blocks (20%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		176.0 MHz 22.5 Gbps	211.0 MHz 27.0 Gbps	241.0 MHz 30.8 Gbps

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 128 bits. The codec throughput of 10.7 Gbps requires a timing frequency of at least 85 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker.

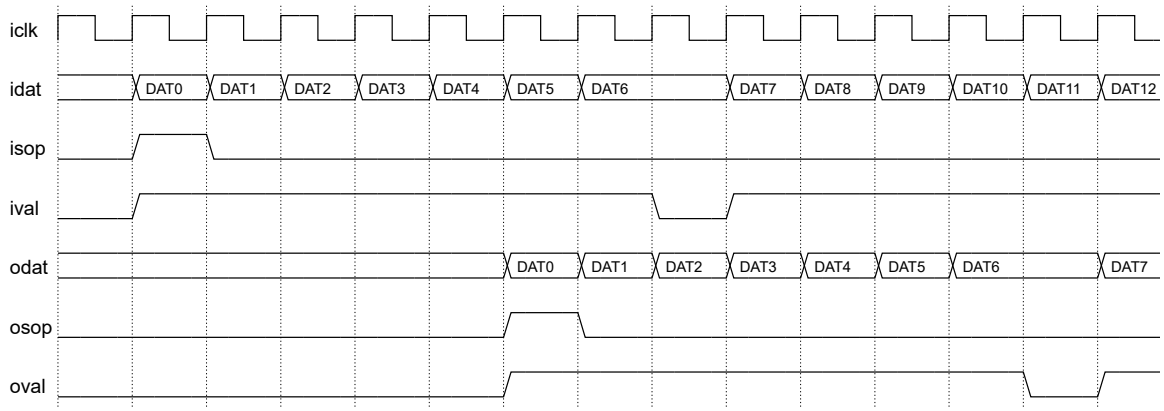

Figure 5. The timing diagrams of the I.3 BCH Encoder operation

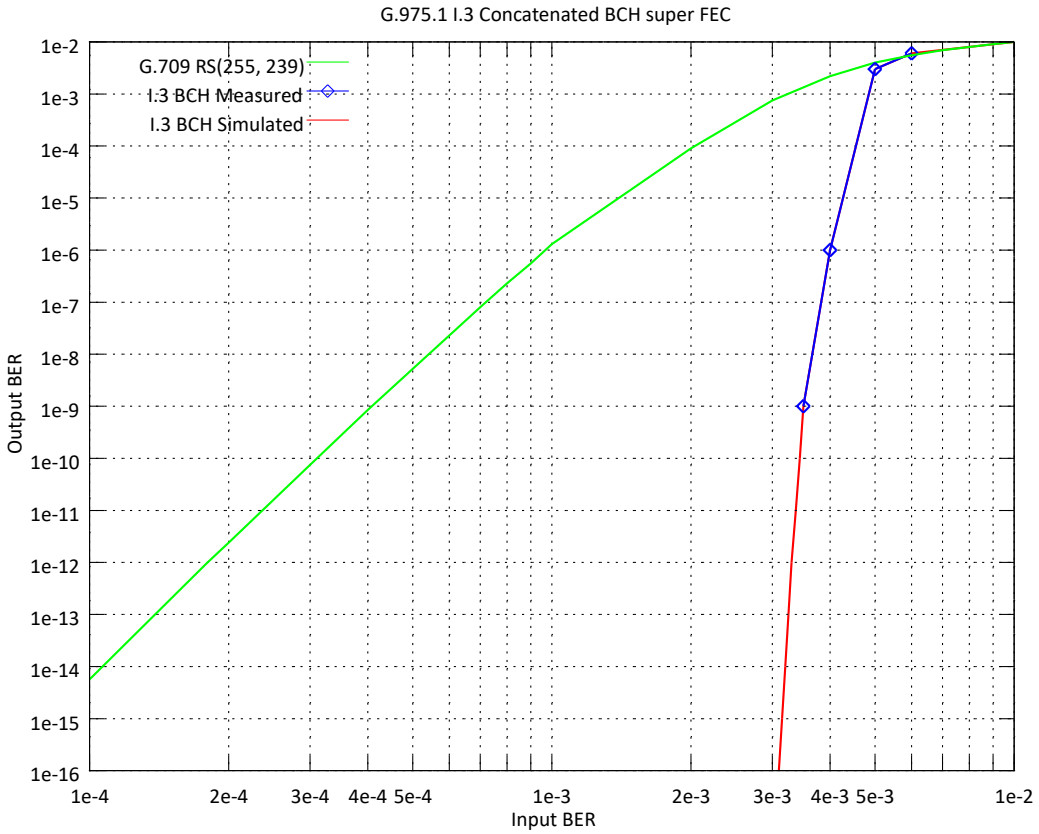

Figure 6. The error-correcting capability of the I.3 BCH Decoder

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

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Revision history

Version	Date	Changes
2.1	2015.09.30	Maintenance improvements
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.0	2012.11.20	Official release