I.6 40G LDPC Encoder/Decoder IP Core Specification

Release Information

Name	I.6 40G LDPC Codec IP Core
Version	1.0
Build date	2017.05
Ordering code	ip-i6-40g-ldpc-codec
Specification revision	r1884

Features

The IP core implements the LDPC (32640, 30592) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.975.1 (super-FEC for 2.5G, 10G and 40G optical networks)

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The I.6 40G LDPC Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the I.6 40G LDPC Encoder IP Core block diagram.

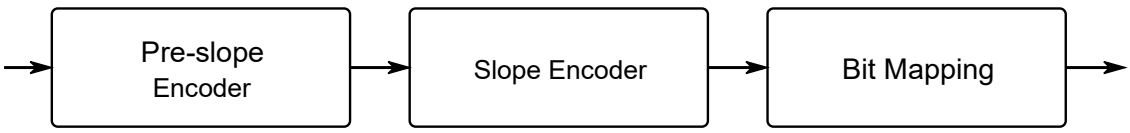

Figure 1. The I.6 40G LDPC Encoder IP Core block diagram

The I.6 40G LDPC Encoder consists of a Pre-slope Encoder module (**Pre-slope Encoder**), a Slope Encoder module (**Slope Encoder**) and a Bit Mapping module (**Bit Mapping**).

Figure 2 shows a block diagram of one I.6 40G LDPC Decoder IP Core decoding iteration.

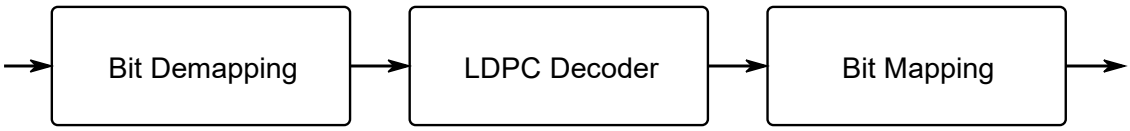

Figure 2. Block diagram of one I.6 40G LDPC Decoder iteration

The I.6 40G LDPC Decoder architecture makes it possible to specify a random number of decoding iterations. A decoding iteration consists of a Bit Demapping module (**Bit Demapping**), a LDPC Decoder module (**LDPC Decoder**) and a Bit Mapping module (**Bit Mapping**).

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the I.6 40G LDPC Encoder IP Core.

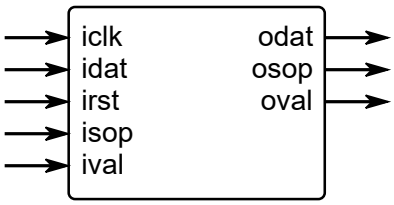

Figure 3. The I.6 40G LDPC Encoder port map

Table 1. The I.6 40G LDPC Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	256	input (information) data
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of information packet marker
ival	1	input data valid
odat	256	output (encoded) data
osop	1	start of encoded packet marker
oval	1	output data valid

Figure 4 shows a graphic symbol, and Table 2 gives a description of the I.6 40G LDPC Decoder IP Core ports.

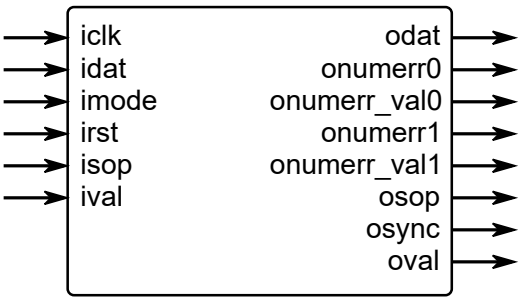

Figure 4. The I.6 40G LDPC Decoder port map

Table 2. The I.6 40G LDPC Decoder port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	256	input (encoded) data
imode	1	decoded data output mode: 0 - without correction (bypass) 1 - with error correction
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of coded packet marker
ival	1	input data valid
odat	256	output (decoded) data
onumerr0	5	number of input blocks with errors
onumerr_val0	1	onumerr0 valid
onumerr1	5	number of output blocks with errors
onumerr_val1	1	onumerr1 valid
osop	1	start of decoded packet marker
osync	1	correct isop with FAS input
oval	1	output data valid

IP Core Operation Description

The I.6 40G LDPC Encoder/Decoder IP Core is in full accordance with the recommendation ITU-T G.975.1 (02/2004) "Appendix I. Super FEC schemes. I.6 40G LDPC super FEC code". The IP Core is designed for operation with the OTN OTU3 linear stream at 43.01 Gbps in fiber optic communication systems. The I.6 40G LDPC Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.975.1 I.6 40G
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 1,020 cycles (6 us)
- Decoding delay of 15 iterations (15 slope decoding) is 2,048 cycles (12 us)

IP Core Parameters

Table 3 describes the I.6 40G LDPC Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The I.6 40G LDPC Encoder/Decoder IP Core parameters description	
Parameter	Description
ITER	number of decoding iterations
s1, ..., s7	slope coefficients

Example:

- ITER = 5 means five iterative decoding iterations:

idat - dec1 - dec2 - dec3 - dec4 - dec5 - odat

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the I.6 40G LDPC Encoder IP Core measurement results.

Table 4. The I.6 40G LDPC Encoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
40G mode	Altera Cyclone IV EP4CE115			
	- LEs - M9K	-3, Fmax	-2, Fmax	-1, Fmax
		—	—	—
40G mode	Xilinx Virtex-6 XC6VLX240T			
	- Slices - 18K RAM blocks	-1, Fmax	-2, Fmax	-3, Fmax
		—	—	—

Table 5 summarizes the I.6 40G LDPC Decoder IP Core measurement results.

Table 5. The I.6 40G LDPC Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
40G mode 15 iterations	Altera Arria 10 10AX066			
	74434 ALMs (30%) 128 M20K RAM blocks (6%) 0 DSP (18x18) (0%)	-3, Fmax	-2, Fmax	-1, Fmax
		190.0 MHz 48.6 Gbps	220.0 MHz 56.3 Gbps	250.0 MHz 64.0 Gbps
40G mode 15 iterations	Xilinx Virtex-7 XC7VX690T			
	27940 Slices (25%) 144 18K RAM blocks (5%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		200.0 MHz 51.2 Gbps	230.0 MHz 58.8 Gbps	260.0 MHz 66.56 Gbps

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 256 bits. The codec throughput of 43.01 Gbps requires a timing frequency of at least 170 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker.

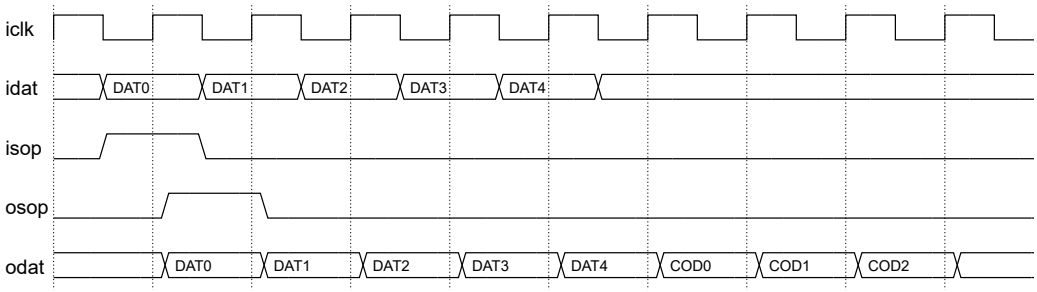

Figure 5. The timing diagrams of the I.6 40G LDPC Encoder operation

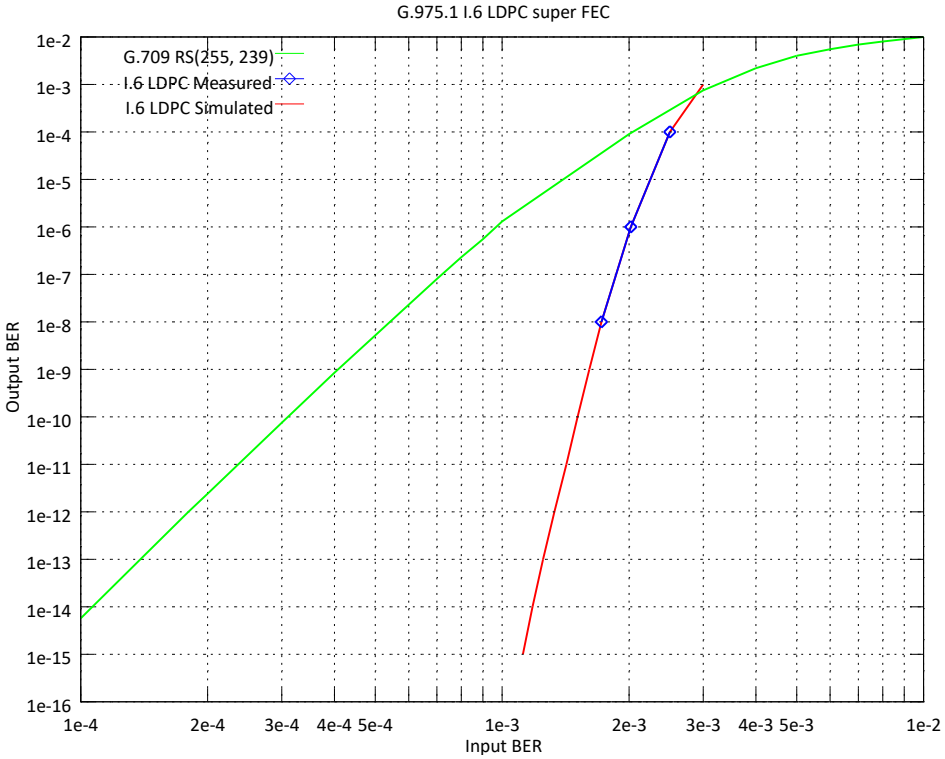

Figure 6. The error-correcting capability of the I.6 40G LDPC Decoder

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

Modemica OU

Sepapaja 6, Tallinn, 15551, Estonia

Tel.: +39-350-0080495

E-mail: info@modemica.com

Skype: fpgahelp

website: https://www.modemica.com

Revision history

Version	Date	Changes
1.0	2017.05.23	Official release