



Multi-gigabit Modem IP Core  
Specification

## Release Information

|                        |                             |
|------------------------|-----------------------------|
| Name                   | Multi-gigabit Modem IP Core |
| Version                | 2.0                         |
| Build date             | 2016.05                     |
| Ordering code          | ip-multi-gigabit-modem      |
| Specification revision | r1884                       |

## Features

The IP core implements full-featured digital QPSK/BPSK modem with Ethernet interface and Reed-Solomon FEC and is intended for E-band wideband microwave communication systems operating in continuous mode.

## License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

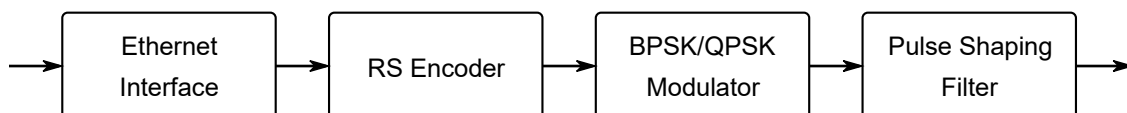
## Deliverables

The Multi-gigabit Modem IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

## IP Core Structure

Figure 1 shows the Multi-gigabit Modulator IP Core block diagram.



**Figure 1. The Multi-gigabit Modulator IP Core block diagram**

Figure 2 shows the Multi-gigabit Demodulator IP Core block diagram.

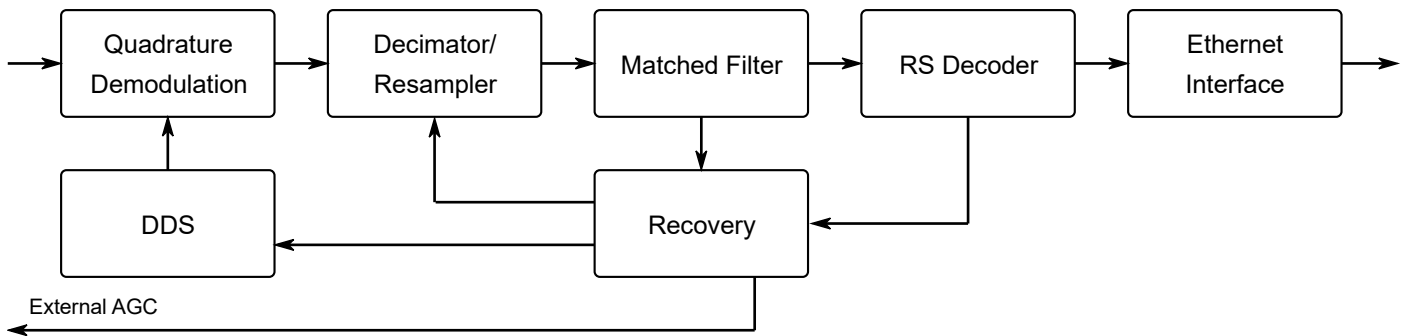


Figure 2. The Multi-gigabit Demodulator IP Core block diagram

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the Multi-gigabit Modulator IP Core.

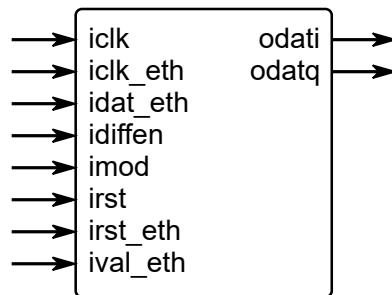
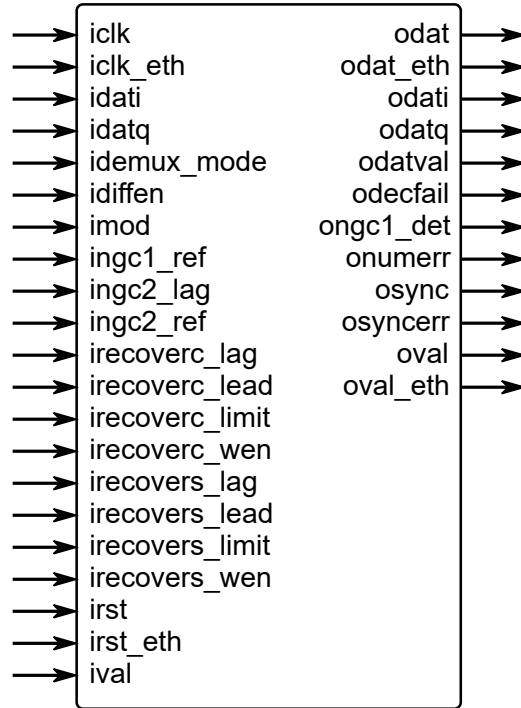


Figure 3. The Multi-gigabit Modulator port map

| Table 1. The Multi-gigabit Modulator port map description |         |   |
|---|---------|---|
| Port  | Width   | Description   |
| iclk  | 1       | The main system clock. The IP Core operates on the rising edge of iclk. |
| iclk_eth  | 1       | Ethernet clock.   |
| idat_eth  | 8 or 16 | Input Ethernet data.  |
| idiffen   | 1       | Enables differential encoding.  |
| imod  | 1       | Modulation:<br>0 - BPSK<br>1 - QPSK                                     |
| irst  | 1       | The IP Core synchronously reset when irst is asserted high.             |
| irst_eth  | 1       | The Ethernet FIFO synchronously reset when irst_eth is asserted high.   |
| ival_eth  | 1       | Valid for input Ethernet data.  |

|                |            |   |
|----------------|------------|---|
| odati<br>odatq | W_DAC*NSPC | Modulator complex IQ output at baseband or at intermediate frequency. |
|----------------|------------|---|

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the Multi-gigabit Demodulator IP Core.



**Figure 4. The Multi-gigabit Demodulator port map**

| Table 2. The Multi-gigabit Demodulator port map description |            |   |
|---|------------|---|
| Port  | Width      | Description   |
| iclk  | 1          | The main system clock. The IP Core operates on the rising edge of iclk. |
| iclk_eth  | 1          | Ethernet clock.   |
| idati   | W_ADC*NSPC | Input data (I-channel) at zero IF.                                      |
| idatq   | W_ADC*NSPC | Input data (Q-channel) at zero IF.                                      |
| idemux_mode   | 2          | Direct connection to the Demodulator data.                              |
| idiffen   | 1          | Enables differential encoding.  |
| imod  | 1          | Set modulation scheme (0-BPSK / 1-QPSK).                                |

|                 |            |   |
|-----------------|------------|---|
| ingc1_ref       | 10         | Setting the reference level of external AGC.                        |
| ingc2_lag       | 3          | Setting the recovery rate of internal AGC.                          |
| ingc2_ref       | 8          | Setting the reference level of internal AGC.                        |
| irecoverc_lag   | 5          | Selecting band loop filter to adjust carrier frequency.             |
| irecoverc_lead  | 5          | Selecting band loop filter to adjust carrier frequency.             |
| irecoverc_limit | 5          | Setting the range of changes to adjust carrier frequency.           |
| irecoverc_wen   | 1          | Enables the loop filter to adjust carrier frequency.                |
| irecoverc_lag   | 5          | Selecting band loop filter to adjust symbol frequency.              |
| irecoverc_lead  | 5          | Selecting band loop filter to adjust symbol frequency.              |
| irecoverc_limit | 5          | Setting the range of changes to adjust symbol frequency.            |
| irecoverc_wen   | 1          | Enables the loop filter to adjust symbol frequency.                 |
| irst            | 1          | The IP Core synchronously reset when irst is asserted high.         |
| irst_eth        | 1          | The output FIFO synchronously reset when irst_eth is asserted high. |
| ival            | 1          | Valid for input data.   |
| odat            | NSPC       | Output (channel) data   |
| odat_eth        | 8 or 16    | Output Ethernet data.   |
| odati           | W_ADC*NSPC | Output constellation (I-channel).                                   |
| odatq           | W_ADC*NSPC | Output constellation (Q-channel).                                   |
| odatval         | 1          | odat valid signal.  |

|           |    |  |
|-----------|----|--|
| odecfail  | 24 | Counter of RS Codec decoding failed events.      |
| ongc1_det | 1  | External AGC detector output.                    |
| onumerr   | 24 | Counter of RS Codec Symbol errors.               |
| osync     | 8  | Counter of 0x47 preamble synchronization errors. |
| osyncerr  | 1  | Error in preamble acquisition.                   |
| oval      | 1  | odati/odatq valid signal.                        |
| oval_eth  | 1  | odat_eth valid signal.                           |

### IP Core Operation Description

Key features of the IP Core:

- Parallel processing for wideband applications. **NSPC** parameter controls degree of parallel
- Synchronous, high-speed algorithm for the formation BPSK/QPSK signals
- Symbol rate is equal to the system clock frequency \* NSPS/4
- Support robust Reed-Solomon FEC
- Fully digital reference frequencies recovery and signal demodulation
- Ethernet interface support
- Fixed delay in modulator and demodulator

IP Core Parameters

Table 3 describes the Multi-gigabit Modem IP Core parameters, which must be set before synthesis.

| Table 3. The Multi-gigabit Modem IP Core parameters description |   |
|---|---|
| Parameter   | Description   |
| NSPC  | <b>Number of Samples Per Cycle.</b> Degree of parallel processing.                                    |
| W_ADC   | <b>ADC Width.</b> Width of the Demodulator input samples from ADC (idati/idatq).                      |
| W_DAC   | <b>DAC Width.</b> Width of the Modulator output samples to DAC (odati/odatq).                         |
| RS(N, K)  | <b>Reed-Solomon Codec.</b> Information block length K and coded block length N of Reed-Solomon Codec. |

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the Multi-gigabit Modulator IP Core measurement results.

| Table 4. The Multi-gigabit Modulator performance |   |                                       |                            |                            |
|--|---|---------------------------------------|----------------------------|----------------------------|
| IP Core parameters                               | FPGA type   |                                       |                            |                            |
|  | Resource  | Speed grade, maximal system frequency |                            |                            |
| NSPC = 12<br>W_DAC = 10<br>RS (204, 188)         | Altera Cyclone V 5CEFA7   |                                       |                            |                            |
|  | 2042 ALMs (1%)<br>7 M10K RAM block (1%)<br>0 DSP (18x18) (0%)   | -8, Fmax                              | -7, Fmax                   | -6, Fmax                   |
|  |   | 154.0 MHz<br>851.5 Mbit/s             | 175.0 MHz<br>967.6 Mbit/s  | 205.0 MHz<br>1133.5 Mbit/s |
| NSPC = 12<br>W_DAC = 10<br>RS (204, 188)         | Xilinx Virtex-7 XC7VX330T                                       |                                       |                            |                            |
|  | 437 Slices (1%)<br>28 18K RAM blocks (2%)<br>0 DSP (18x18) (0%) | -1, Fmax                              | -2, Fmax                   | -3, Fmax                   |
|  |   | 282.0 MHz<br>1559.3 Mbit/s            | 360.0 MHz<br>1990.0 Mbit/s | 380.0 MHz<br>2101.0 Mbit/s |

Table 5 summarizes the Multi-gigabit Demodulator IP Core measurement results.



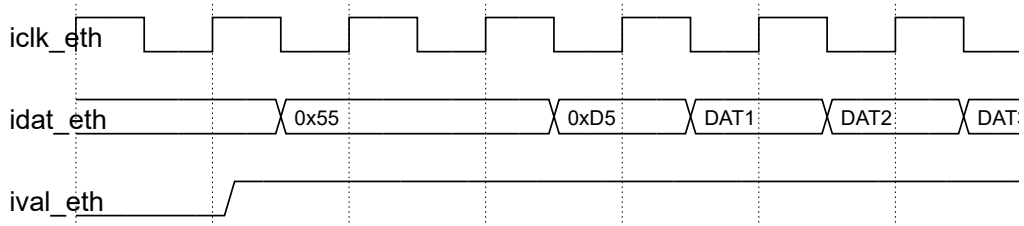
| Table 5. The Multi-gigabit Demodulator performance |  |                                       |                            |                            |
|--|--|---------------------------------------|----------------------------|----------------------------|
| IP Core parameters                                 | FPGA type  |                                       |                            |                            |
|  | Resource   | Speed grade, maximal system frequency |                            |                            |
| NSPC = 12<br>W_ADC = 10<br>RS (204, 188)           | Altera Cyclone V 5CEFA7  |                                       |                            |                            |
|  | 14442 ALMs (26%)<br>10 M10K RAM block (2%)<br>50 DSP (18x18) (32%) | -8, Fmax                              | -7, Fmax                   | -6, Fmax                   |
|  |  | 80.0 MHz<br>442.3 Mbit/s              | 96.0 MHz<br>530.8 Mbit/s   | 108.0 MHz<br>597.1 Mbit/s  |
| NSPC = 12<br>W_ADC = 10<br>RS (204, 188)           | Xilinx Virtex-7 XC7VX330T  |                                       |                            |                            |
|  | 8210 Slices (16%)<br>7 18K RAM blocks (1%)<br>48 DSP (18x18) (5%)  | -1, Fmax                              | -2, Fmax                   | -3, Fmax                   |
|  |  | 196.0 MHz<br>1083.7 Mbit/s            | 240.0 MHz<br>1327.0 Mbit/s | 262.0 MHz<br>1448.7 Mbit/s |

Table 6 shows the modem performance with respect to NSPC parameter for FPGA Xilinx Virtex-7 speed grade -2.

| Table 6. Modem performance with respect to NSPC parameter |        |      |     |      |                     |                  |              |
|---|--------|------|-----|------|---------------------|------------------|--------------|
| NSPC  | Slices | BRAM | DSP | Fmax | ADC/DAC Sample rate | QPSK Symbol rate | Data bitrate |
| 4   | 3748   | 23   | 16  | 300  | 1200 or 600 MSPS    | 300 Msym/s       | 600 Mbit/s   |
| 8   | 6202   | 31   | 32  | 260  | 2080 or 1040 MSPS   | 520 Msym/s       | 1040 Mbit/s  |
| 12  | 8660   | 39   | 48  | 240  | 2880 or 1440 MSPS   | 720 Msym/s       | 1440 Mbit/s  |
| 16  | 11485  | 47   | 64  | 230  | 3680 or 1840 MSPS   | 920 Msym/s       | 1840 Mbit/s  |
| 20  | 14112  | 55   | 80  | 220  | 4400 or 2200 MSPS   | 1100 Msym/s      | 2200 Mbit/s  |
| 24  | 17292  | 63   | 96  | 210  | 5040 or 2520 MSPS   | 1260 Msym/s      | 2520 Mbit/s  |
| 32  | 22778  | 79   | 128 | 155  | 4960 or 2480 MSPS   | 1240 Msym/s      | 2480 Mbit/s  |
| 40  | 27982  | 95   | 160 | 120  | 4800 or 2400 MSPS   | 1200 Msym/s      | 2400 Mbit/s  |
| 64  | 49284  | 143  | 256 | 70   | 4480 or 2240 MSPS   | 1120 Msym/s      | 2240 Mbit/s  |

IP Core Interface Description

Figure 5 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").



**Figure 5. The timing diagrams of the Multi-gigabit Modulator operation**

### Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.modemica.com/>

### Feedback

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### Revision history

| Version | Date       | Changes                          |
|---------|------------|----------------------------------|
| 2.0     | 2016.05.03 | Added Ethernet interface support |
| 1.0     | 2015.10.20 | Official release                 |