QAM Demodulator IP Core Specification

Release Information

Name	QAM Demodulator IP Core
Version	3.0
Build date	2014.09
Ordering code	ip-qam-demodulator
Specification revision	r1884

Features

The IP core implements the full-featured QAM demodulation algorithm and is fully compatible with those standards:

- Digital Video Broadcasting (DVB-S, DVB-C, DVB-S2)
- ITU-T for point-to-point microwave communication systems

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The QAM Demodulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the QAM Demodulator IP Core block diagram.

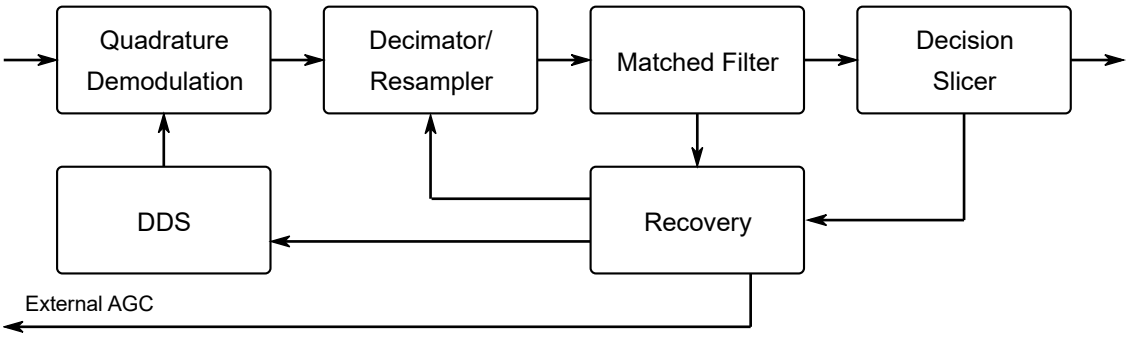

Figure 1. The QAM Demodulator IP Core block diagram

The QAM demodulator consists of a quadrature demodulator (**Quadrature Demodulation**), a direct digital synthesis module

(**Direct Digital Synthesis**), a decimator/fractional resampler (**Resampler**), a RRC filter (**Matched Filter**), a decision slicer (**Decision Slicer**), a carrier frequency, a symbol clock recovery and an AGC control module (**Recovery**).

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the QAM Demodulator IP Core.

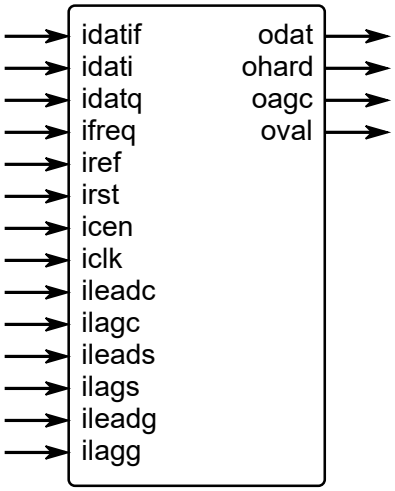

Figure 2. The QAM Demodulator port map

Table 1. The QAM Demodulator port map description

Port	Width	Description
idatif	W_IN	demodulator input at intermediate frequency
idati	W_IN	demodulator input at baseband (I channel)
idatq	W_IN	demodulator input at baseband (Q channel)
ifreq	32	reference frequency for carrier recovery
iref	16	reference gain for AGC recovery
irst	1	The IP Core synchronously reset when irst is asserted high.
icen	1	input data valid
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.

ileadc, ilagc	5	carrier recovery loop filter bandwidth
ileads, ilags	5	symbol recovery loop filter bandwidth
ileadg, ilagg	5	gain recovery loop filter bandwidth
odat	W_OUT	soft decision for demodulated signal
ohard	8	hard decision for demodulated signal
oagc	1	external AGC control PWM output
oval	1	output data valid

IP Core Operation Description

For correct recovery of QAM-modulated signal at the receiver must be known with an accuracy of carrier phase and symbol rate. To adjust the carrier most advanced QAM demodulators use different versions of the classical scheme Costas, and to adjust the clock speed - the scheme Gardner. The main criterion is the quality of the algorithms adjust the threshold signal / noise ratio at which the recovery occurs with the required quality.

Key features of the IP Core:

- Fully digital QAM signal coherent demodulation
- Intermediate frequency input range up to 40% of the system clock frequency
- Digital restoration of character frequency (without external VCXO)
- Symbol rate to 1/4 of the system clock frequency
- Support for changing demodulation schemes "on the fly"
- Parameterized receiving matched filter and decimator
- Fixed delay in the demodulator

IP Core Parameters

Table 2 describes the QAM Demodulator IP Core parameters, which must be set before synthesis.

Table 2. The QAM Demodulator IP Core parameters description

Parameter	Description
W_IN	Width of input data (ADC resolution)
W_OUT	Widht of output soft decision symbols
MOD	Highest modulation type, for example "1024QAM"
ROLL-OFF	Roll-off factor (alpha) of shaping filter (RRC).
DEMIXER_MOD	demixer mode, for example "IF" or "BASEBAND"
L	Decimation coefficient

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the QAM Demodulator IP Core measurement results.

Table 3. The QAM Demodulator performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
1024QAM W_IN=12 DEMIXER_MOD ="VIDEO" L=4 ROLL- OFF=25%	Altera Cyclone II EP2C35			
	16,406 LEs 90,112 bits 20 DSP blocks (9x9)	-8, Fmax	-7, Fmax	-6, Fmax
		168.0 MHz 42.0 Msymb/s	186.0 MHz 46.5 Msymb/s	216.0 MHz 54.0 Msymb/s
1024QAM W_IN=12 DEMIXER_MOD ="VIDEO" L=4 ROLL- OFF=25%	Xilinx Spartan-3A DSP XC3SD1800			
	9,143 slices 90,112 bits (16 BRAMs) 9 DSP blocks (18x18)	-4, Fmax	-5, Fmax	
		110.0 MHz 27.5 Msymb/s	144.0 MHz 36.0 Msymb/s	

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

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Revision history

Version	Date	Changes
3.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
2.1	2010.05.04	Maintenance improvements
2.0	2009.08.18	Added 16-APSK/32-APSK/64-APSK modulation support
1.2	2008.10.10	Added 256-QAM/1024-QAM modulation support
1.1	2008.06.04	Added 64-QAM modulation support
1.0	2007.03.06	Official release