RS-QPSK Modem IP Core Specification

Release Information

Name	RS-QPSK Modem IP Core
Version	2.1
Build date	2018.02
Ordering code	ip-rs-qpsk-modem
Specification revision	r1884

Features

The IP core implements full-featured digital QPSK/BPSK modem with Reed-Solomon FEC and is intended for satellite and microwave communication systems operating in continuous mode.

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The RS-QPSK Modem IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the RS-QPSK Modulator IP Core block diagram.

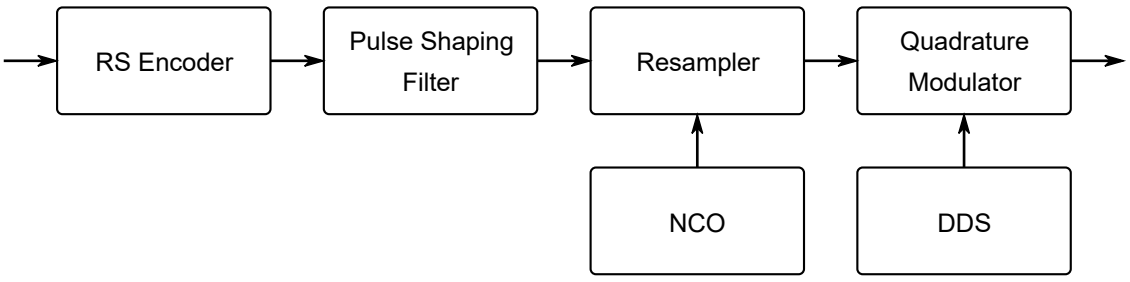

Figure 1. The RS-QPSK Modulator IP Core block diagram

The RS-QPSK Modulator consists of a Reed-Solomon encoder and a BPSK/QPSK modulator.

Figure 2 shows the RS-QPSK Demodulator IP Core block diagram.

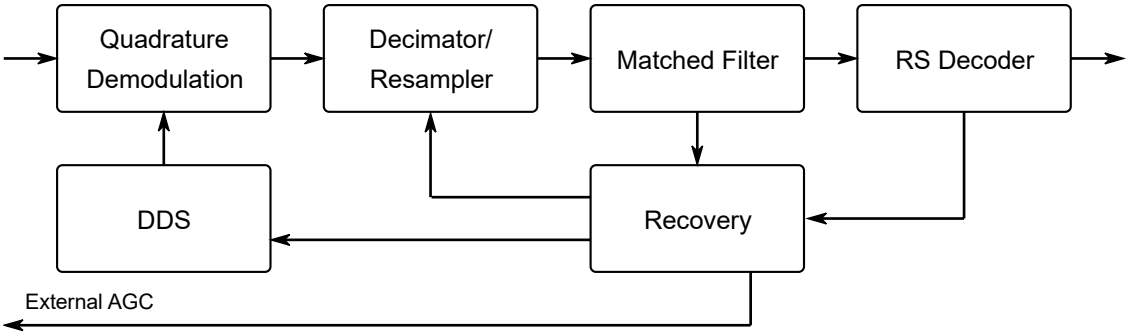

Figure 2. The RS-QPSK Demodulator IP Core block diagram

The RS-QPSK Demodulator consists of a BPSK/QPSK demodulator and a Reed-Solomon decoder.

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the RS-QPSK Modulator IP Core.

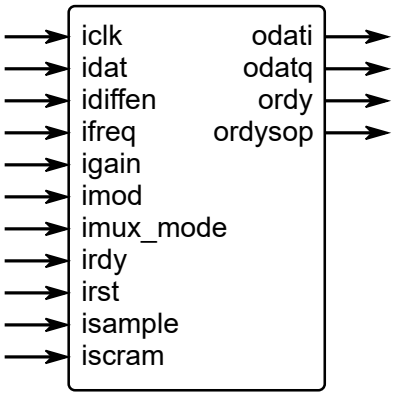

Figure 3. The RS-QPSK Modulator port map

Table 1. The RS-QPSK Modulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	8	Input (information) data.
idiffen	1	Enables differential encoding.
ifreq	32	Output intermediate frequency.
igain	16	Output gain control.
imod	1	Modulation: 0 - BPSK 1 - QPSK

imux_mode	2	Data mux mode: 0 - RS Coder + SYNCBYTE 1 - SYNCBYTE only 2 - Direct access
irdy	1	Modulator output data request.
irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	Bandwidth control (symbol rate): 0.01% to 25% of iclk.
iscram	1	Enables internal data scrambler.
odati odatq	W_DAC	Modulator complex IQ output at baseband or at intermediate frequency.
ordy	1	Ready to accept input data.
ordysop	1	Ready to accept **isop** and start new RS block.

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the RS-QPSK Demodulator IP Core.

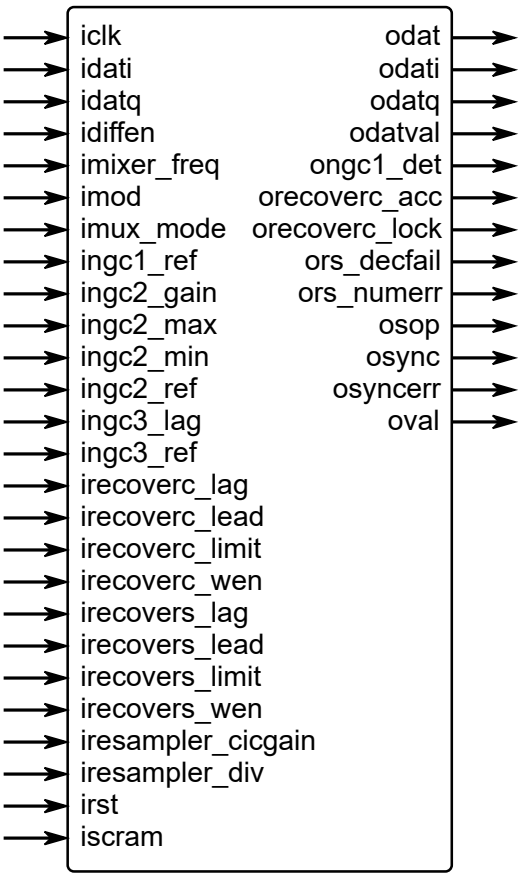

Figure 4. The RS-QPSK Demodulator port map

Table 2. The RS-QPSK Demodulator port map description

Port	Width	Description
iclk	1	System clock frequency
idati	W_ADC	Input data (I-channel) at zero IF
idatq	W_ADC	Input data (Q-channel) at zero IF
idiffen	1	Enables differential encoding
imixer_freq	32	Setup input intermediate frequency
imod	1	Set modulation scheme (0-BPSK / 1-QPSK)
imux_mode	2	Data mux mode: 0 - RS Coder + SYNCBYTE 1 - SYNCBYTE only 2 - Direct access
ingc1_ref	10	Setting the reference level of external AGC

ingc2_gain	8	Adjust the speed of adjustment of internal AGC
ingc2_max	16	Set maximum level of AGC
ingc2_min	16	Set minimum level of AGC
ingc2_ref	10	Setting the reference level of internal AGC
ingc3_lag	3	Setting the reference level of internal AGC
ingc3_ref	8	Setting the reference level of internal AGC
irecoverc_lag	5	Selecting band loop filter to adjust carrier frequency
irecoverc_lead	5	Selecting band loop filter to adjust carrier frequency
irecoverc_limit	5	Setting the range of changes to adjust carrier frequency
irecoverc_wen	1	Enables the loop filter to adjust carrier frequency
irecoverc_lag	5	Selecting band loop filter to adjust symbol frequency
irecoverc_lead	5	Selecting band loop filter to adjust symbol frequency
irecoverc_limit	5	Setting the range of changes to adjust symbol frequency
irecoverc_wen	1	Enables the loop filter to adjust symbol frequency
iresampler_cicgain	6	CIC Filter gain control
iresampler_div	12	CIC Filter decimation ratio
irst	1	The IP Core synchronously reset when irst is asserted high.
iscram	1	Enables internal data scrambler.
odat	8	Output (Information) data
odati	8	Output constellation (I-channel)

odatq	8	Output constellation (Q-channel)
odatval	1	odat valid signal
ongc1_det	1	External AGC detector output
orecoverc_acc	32	Carrier frequency error value
orecoverc_lock	2	Carrier frequency lock indicator
ors_decfail	1	RS Codec decoding failed
ors_numerr	4	RS Codec number of detected errors in single block
osop	1	RS Codec start of decoding block
osync	1	0x47 preamble correct acquisition
osyncerr	1	Error in preamble acquisition
oval	1	odati/odatq valid signal

IP Core Operation Description

Key features of the IP Core:

- Synchronous, high-speed algorithm for the formation BPSK/QPSK signals
- The output of the intermediate frequency range up to 40% of the system clock frequency
- Symbol rate to 1/4 of the system clock frequency
- Support robust Reed-Solomon FEC
- Fully digital reference frequencies recovery and signal demodulation
- Fixed delay in modulator and demodulator

IP Core Parameters

Table 3 describes the RS-QPSK Modem IP Core parameters, which must be set before synthesis.

Table 3. The RS-QPSK Modem IP Core parameters description

Parameter	Description
W_ADC	**ADC Width**. Width of the Demodulator input samples from ADC (**idati/idatq**).
W_DAC	**DAC Width**. Width of the Modulator output samples to DAC (**odati/odatq**).
RS(N, K)	**Reed-Solomon Codec**. Information block length **K** and coded block length **N** of Reed-Solomon Codec.

Setting Port Parameters

Some input ports that control the IP Core operation need to be set to suit custom configuration.

Carrier frequency:

$$ifreq = \frac{Output\ \ Frequency(Hz)}{iclk\ \ rate(Hz)} \cdot 2^{32}$$

Symbol rate:

$$isample = \frac{Output\ \ Symbol\ \ rate(Hz)}{iclk\ \ rate(Hz)} \cdot 2^{34}$$

Output gain:

$$igain = 8192 \cdot (10^{\frac{Output\ gain(db)}{20}} - 1)$$

Carrier frequency lock range:

$$Limit\ \ Factor = 2^{30 - irecoverc\_limit}$$

$$Single\ \ Side\ \ Range\ (Hz) = \frac{Symbol\ \ Rate\ (Hz)}{Limit\ \ Factor}$$

$$Carrier\ \ Frequency\ \ Range\ \ Limit\ (Hz) = \pm\ Single\ \ Side\ \ Range\ (Hz)$$

Symbol rate lock range:

$$Limit\ Factor = 2^{31 - irecovers\_limit}$$

$$Single\ Side\ Range\ (Hz) = \frac{Symbol\ Rate\ (Hz)}{Limit\ Factor}$$

$$Symbol\ Rate\ Range\ Limit\ (Hz) = \pm\ Single\ Side\ Range\ (Hz)$$

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the RS-QPSK Modulator IP Core measurement results.

Table 4. The RS-QPSK Modulator performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_DAC = 10 RS (204, 188)	Altera Cyclone V 5CEFA7			
	1042 ALMs (1%) 1 M10K RAM block (1%) 12 DSP (18x18) (8%)	-8, Fmax	-7, Fmax	-6, Fmax
		154.0 MHz 70.0 Mbps	175.0 MHz 80.0 Mbps	205.0 MHz 93.0 Mbps
W_DAC = 10 RS (204, 188)	Xilinx Virtex-7 XC7VX330T			
	416 Slices (1%) 1 18K RAM blocks (1%) 12 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		282.0 MHz 129.0 Mbps	360.0 MHz 165.0 Mbps	380.0 MHz 174.0 Mbps

Table 5 summarizes the RS-QPSK Demodulator IP Core measurement results.

Table 5. The RS-QPSK Demodulator performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_ADC = 10 RS (204, 188)	Altera Cyclone V 5CEFA7			
	3655 ALMs (7%) 5 M10K RAM block (1%) 14 DSP (18x18) (9%)	-8, Fmax	-7, Fmax	-6, Fmax
		119.0 MHz 54.0 Mbps	135.0 MHz 61.0 Mbps	152.0 MHz 69.0 Mbps
W_ADC = 10 RS (204, 188)	Xilinx Virtex-7 XC7VX330T			
	2075 Slices (5%) 5 18K RAM blocks (1%) 14 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		189.0 MHz 86.0 Mbps	222.0 MHz 101.0 Mbps	245.0 MHz 112.0 Mbps

IP Core Interface Description

Figure 5 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").

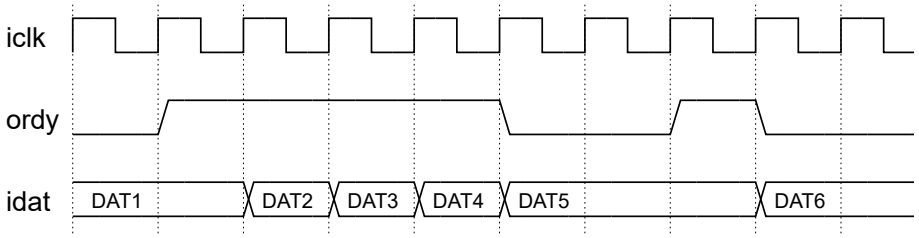

Figure 5. The timing diagrams of the RS-QPSK Modulator operation

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.modemica.com/

Feedback

Modemica OU

Sepapaja 6, Tallinn, 15551, Estonia

Tel.: +39-350-0080495

E-mail: info@modemica.com

Skype: fpgahelp

website: https://www.modemica.com

Revision history

Version	Date	Changes
2.1	2018.02.21	Changed output interface. Added number of errors in RS block indication port
2.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
1.1	2017.07.31	Changed output interface. Added carrier frequency error indication ports
1.0	2015.03.24	Official release