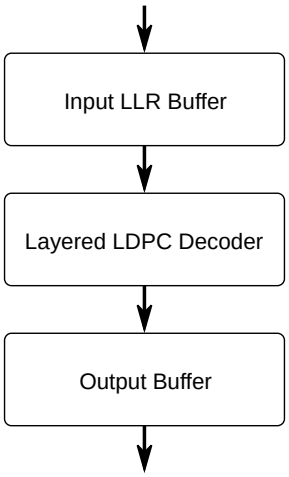
WLAN WiFi LDPC Encoder / Decoder IP Core

IP Core Features

- All code rates
- All block lengths
- High throughput
- Low implementation loss
- Low FPGA resource usage



Key Features

- Compliant with IEEE 802.11n-2009 Standard:
  - Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification
- Supports all WiFi LDPC encoding schemes:
  - 1/2, 2/3, 3/4 and 5/6 code rates
  - 648, 1296 and 1944 block lengths
- On-the-fly block type change
- Layered Min-Sum-Offset decoding with low implementation loss
- Decoding early termination mechanism
- Variable number of decoding iterations up to 256

Applications

- Wireless Local Area Networks (WLAN)
- WiFi modems
- Custom modems with burst/packet mode support
- Systems with the need of powerful LDPC Codes
- FEC for low latency communication systems

Deliverables

- Encrypted Netlist or Complete RTL Source Code versions
- IP Core testbench scripts and design examples for evaluation boards
- Comprehensive integration guide
- Free 1 year technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Royalty-free license without quantitative restrictions
- Off-the-shelf Xilinx and Analog Devices evaluation boards support

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